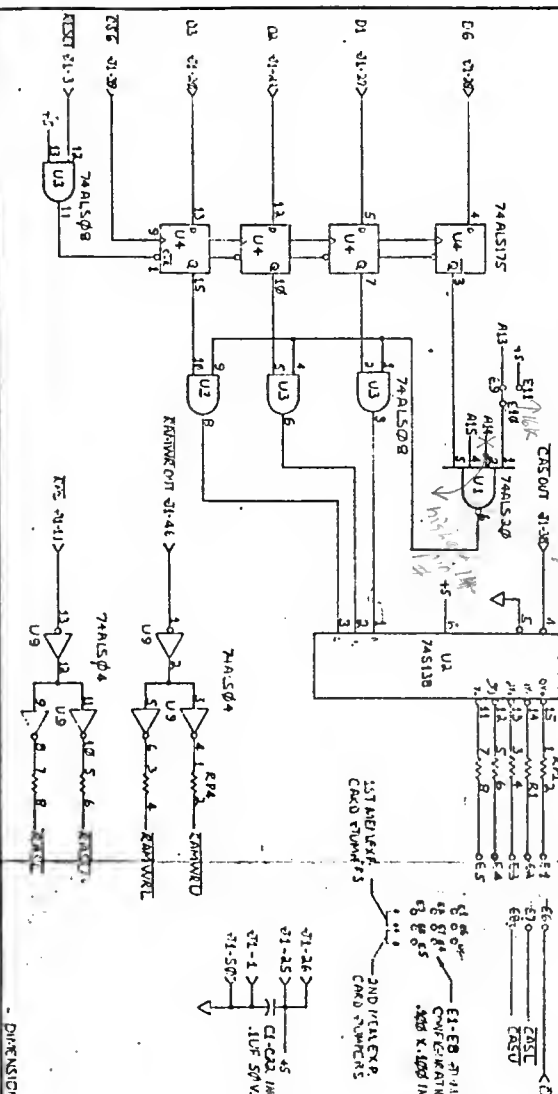
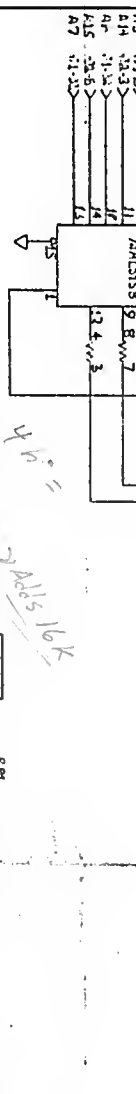


The schematic diagram illustrates the 64K memory bank architecture. An octal decoder (U6, 74ALS08) is driven by address lines A0, A1, A2, and A3. Its outputs (Y0-Y7) are connected to the chip select inputs of eight 64K memory chips (U11-U18). The chips are arranged in two banks of four, with the top bank labeled 'UPPER 64K MEM BANK'. Each chip is connected to address lines A14, A15, A16, and A17, data lines D0 through D7, and control signals RAS, CS, and KAS. The decoder also provides a common ground connection for the memory chips.



MAXIMUM OUTLINE OF  
1180-4000 MHz  
HORN EXPANSION  
CARD

END OF APRIL 21  
800 APRIL-CARD

4.70

0.21

0.22

ALIGN W/ APRIL-CARD P1  
AND W/ APRIL-CARD P2

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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	INITIAL DESIGN AND P.C. BOARD	10-17-82	E.C.
1	FIRST P&ID BOARDS - SHOWER CONTR. CHANGE	12-29-82	R.K.

[illegible]